

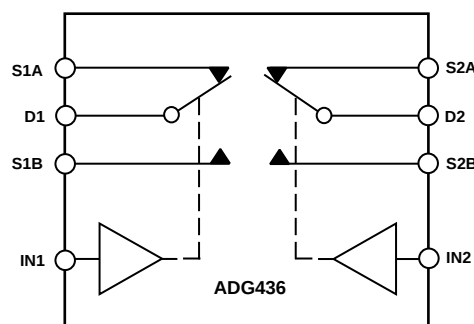
FEATURES

44 V Supply Maximum Ratings
 V_{SS} to V_{DD} Analog Signal Range
Low On Resistance ($12\ \Omega$ Typ)
Low ΔR_{ON} ($3\ \Omega$ Max)
Low R_{ON} Match ($2.5\ \Omega$ Max)
Low Power Dissipation
Fast Switching Times
 $t_{ON} < 175\ ns$
 $t_{OFF} < 145\ ns$
Low Leakage Currents ($5\ nA$ Max)
Low Charge Injection ($10\ pC$)
Break-Before-Make Switching Action

APPLICATIONS

Audio and Video Switching
Battery Powered Systems
Test Equipment
Communications Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG436 is a monolithic CMOS device comprising two independently selectable SPDT switches. It is designed on an LC^2MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable and battery powered instruments.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. **Extended Signal Range**
The ADG436 is fabricated on an enhanced LC^2MOS process, giving an increased signal range which extends to the supply rails.
2. **Low Power Dissipation**
3. **Low R_{ON}**
4. **Single Supply Operation**
For applications where the analog signal is unipolar, the ADG436 can be operated from a single rail power supply.

REV. A

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ADG436—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	+25°C	−40°C to +85°C	Units	Test Conditions/ Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	12	25	Ω typ Ω max	$V_D = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
ΔR_{ON}	1	3	Ω typ Ω max	$V_D = -5\text{ V}$, 5 V , $I_S = -10\text{ mA}$
R_{ON} Match	1	2.5	Ω typ Ω max	$V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.005 ± 0.25	± 5	nA typ nA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$, $V_S = \pm 15.5\text{ V}$ Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.05 ± 0.4	± 5	nA typ nA max	$V_S = V_D = \pm 15.5\text{ V}$ Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}		± 0.005 ± 0.5	μA typ μA max	$V_{IN} = 0\text{ V}$ or V_{DD}
DYNAMIC CHARACTERISTICS²				
t_{ON}	70	125	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
t_{OFF}	60	120	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 5
Charge Injection	10		pC typ	$V_D = 0\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$; Test Circuit 6
OFF Isolation	72		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 2.3\text{ V rms}$, Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 2.3\text{ V rms}$, Test Circuit 8
C_S (OFF)	10		pF typ	
C_D , C_S (ON)	30		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05	0.35	mA typ mA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.01 1	5	μA typ μA max	
V_{DD}/V_{SS}		$\pm 3/\pm 20$	V min/V max	$ V_{DD} = V_{SS} $

NOTES

¹Temperature range is as follows: B Version, -40°C to $+85^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply ($V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	+25°C	−40°C to +85°C	Units	Test Conditions/ Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
R_{ON}	20	40	Ω typ Ω max	$V_D = +1\text{ V}$, $+10\text{ V}$, $I_S = -1\text{ mA}$
R_{ON} Match		2.5	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.005 ± 0.25	± 5	nA typ nA max	$V_{DD} = +13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$ Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.05 ± 4	± 5	nA typ nA max	$V_S = V_D = 12.2\text{ V}/1\text{ V}$ Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}		± 0.005 ± 0.5	μA typ μA max	$V_{IN} = 0\text{ V}$ or V_{DD}
DYNAMIC CHARACTERISTICS²				
t_{ON}	100	200	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4
t_{OFF}	90	180	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 5
Charge Injection	10		pC typ	$V_D = 6\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$; Test Circuit 6
OFF Isolation	72		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 1.15\text{ V rms}$; Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	$R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; $V_S = 1.15\text{ V rms}$; Test Circuit 8
C_S (OFF)	10		pF typ	
C_D , C_S (ON)	30		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05	0.35	mA typ mA max	$V_{DD} = +13.5\text{ V}$ Digital Inputs = 0 V or 5 V
V_{DD}		+3/+30	V min/V max	

NOTES

¹Temperature range is as follows: B Version, −40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG436

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+44 V
V _{DD} to GND	−0.3 V to +30 V
V _{SS} to GND	+0.3 V to −30 V
Analog, Digital Inputs ²	V _{SS} − 2 V to V _{DD} + 2 V or 20 mA, whichever occurs first
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Junction Temperature	+150°C
Plastic DIP Package	
θ _{JA} , Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	+260°C

SOIC Package

θ _{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG436 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. Truth Table

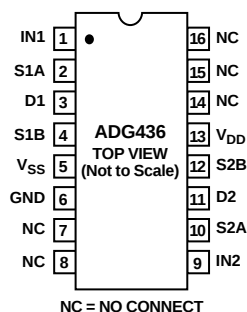
Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
ADG436BN	−40°C to +85°C	Plastic DIP	N-16
ADG436BR	−40°C to +85°C	0.15" SOIC	R-16A

TERMINOLOGY

V_{DD}	Most positive power supply potential.	t_{OFF}	Delay between applying the digital control input and the output switching off.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.	t_{OPEN}	Break-before-make delay when switches are configured as a multiplexer.
GND	Ground (0 V) reference.	V_{INL}	Maximum input voltage for Logic “0.”
S	Source terminal. May be an input or output.	V_{INH}	Minimum input voltage for Logic “1.”
D	Drain terminal. May be an input or output.	I_{INL} (I_{INH})	Input current of the digital input.
IN	Logic control input.	Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
R_{ON}	Ohmic resistance between D and S.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
ΔR_{ON}	R_{ON} variation due to a change in the analog input voltage with a constant load current.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
R_{ON} Match	Difference between the R_{ON} of any two channels.	I_{DD}	Positive supply current.
I_S (OFF)	Source leakage current with the switch “OFF.”	I_{SS}	Negative supply current.
I_D , I_S (ON)	Channel leakage current with the switch “ON.”		
V_D (V_S)	Analog voltage on terminals D, S.		
C_S (OFF)	“OFF” switch source capacitance.		
C_D , C_S (ON)	“ON” switch capacitance.		
t_{ON}	Delay between applying the digital control input and the output switching on.		

PIN CONFIGURATION
(DIP/SOIC)


ADG436—Typical Performance Characteristics

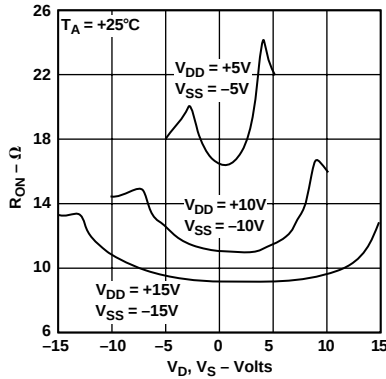


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply

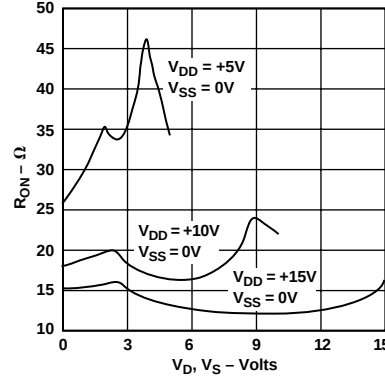


Figure 2. R_{ON} as a Function of V_D (V_S): Single Power Supply

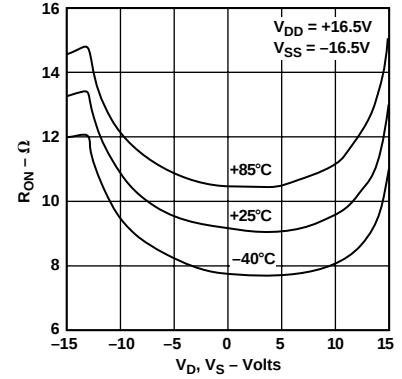


Figure 3. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Dual Supply

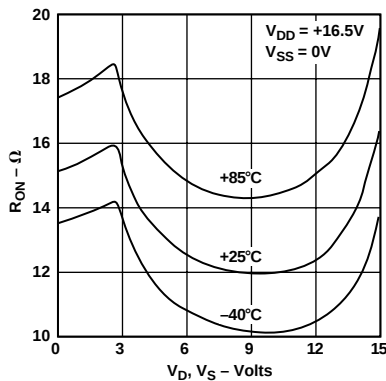


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures: Single Supply

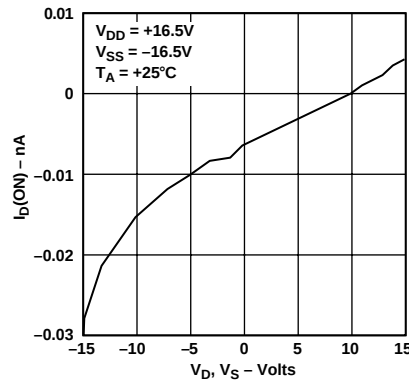


Figure 5. I_D (ON) Leakage Current as a Function of V_D (V_S): Dual Supply

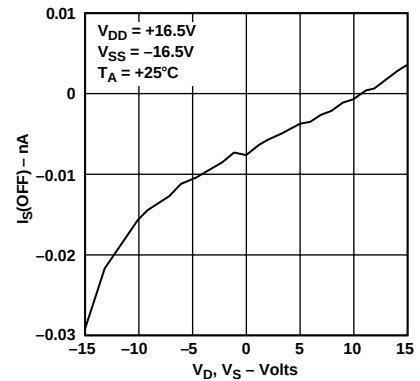


Figure 6. I_S (OFF) Leakage Current as a Function of V_D (V_S): Dual Supply

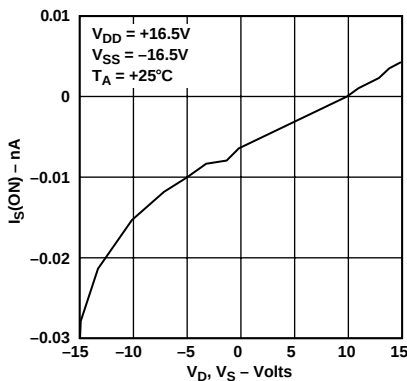


Figure 7. I_S (ON) Leakage Current as a Function of V_D (V_S): Dual Supply

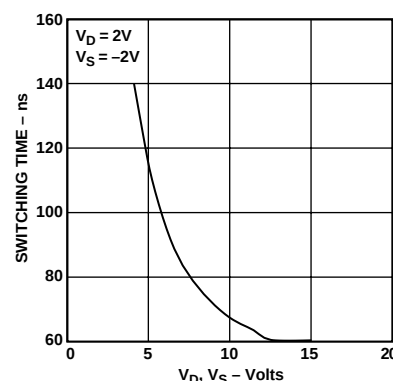


Figure 8. Switching Time as a Function of V_D (V_S): Dual Supply

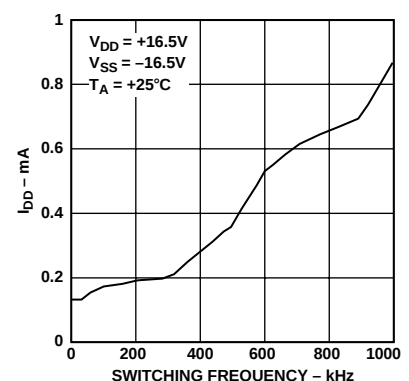
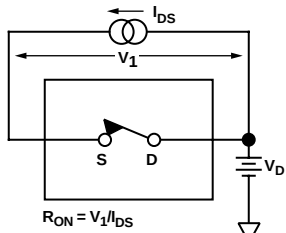
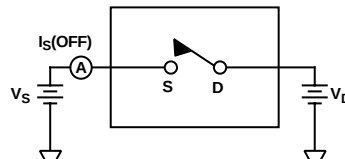


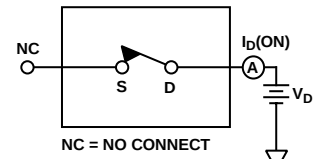
Figure 9. I_{DD} as a Function of Switching Frequency: Dual Supply



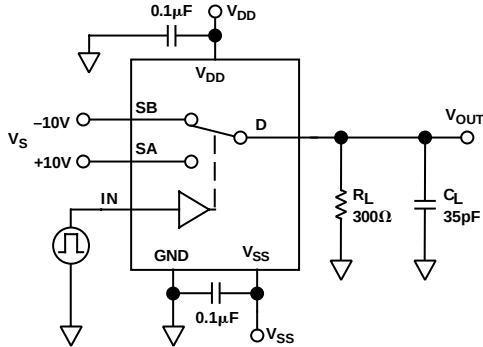
Test Circuit 1. On Resistance



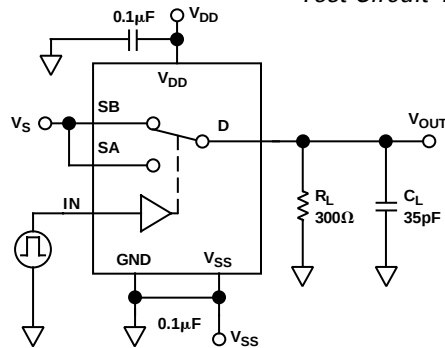
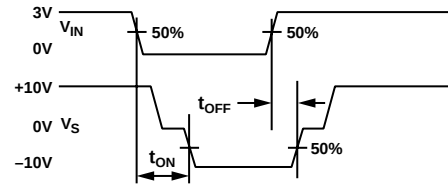
Test Circuit 2. Off Leakage



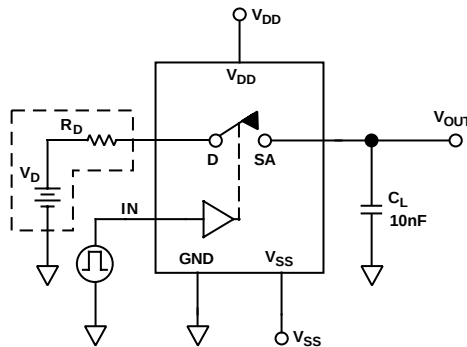
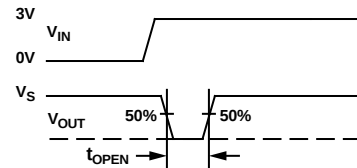
Test Circuit 3. On Leakage



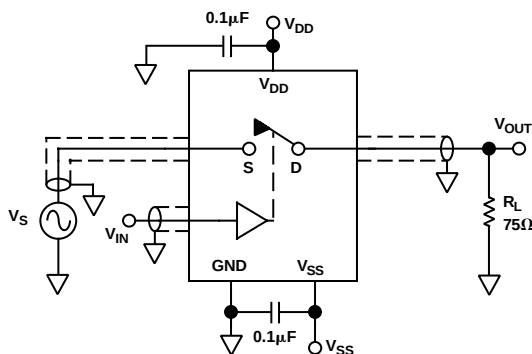
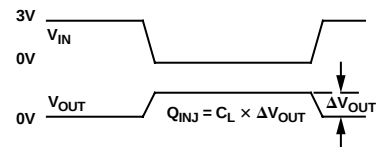
Test Circuit 4. Switching Times



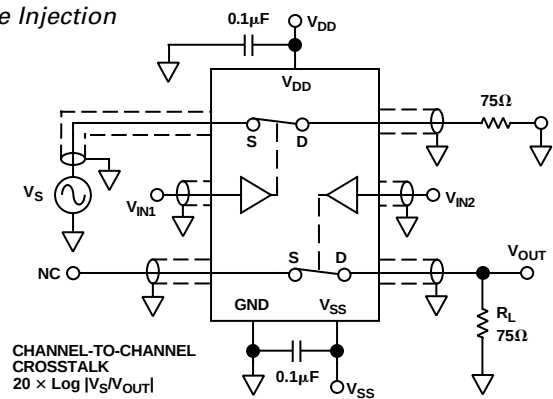
Test Circuit 5. Break-Before-Make Delay, t_{OPEN}



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

